



*Ifw*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicants:** James W. Adkisson, et al

**Examiner:** Unassigned

**Serial No.:** *10/710642*

**Group Art Unit:**

**Filed:** *7-27-04*

**Docket:** BUR920030194US1 (17344)

**For:** DESIGNING SCAN CHAINS WITH SPECIFIC  
PARAMETER SENSITIVITIES TO IDENTIFY  
PROCESS DEFECTS

**Dated:** May 10, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

Applicants are submitting copies of the cited references, along with an English Abstract which explains the pertinence of the reference.

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**CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)**

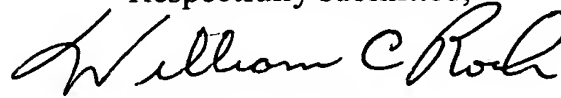
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450 on *7-30-04*.

Dated: *7-30-04*

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Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "William C. Roch". The signature is fluid and cursive, with the first name "William" being the most prominent part.

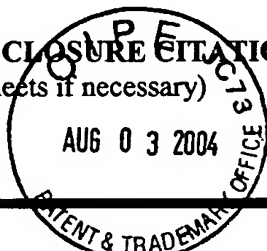
William C. Roch

Registration No.: 24,972

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WCR:jf

**INFORMATION DISCLOSURE CITATION**  
(Use several sheets if necessary)



Docket Number (Optional)  
BUR920030194US1 (17344)

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Applicant(s)  
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**U.S. PATENT DOCUMENTS**

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

**FOREIGN PATENT DOCUMENTS**

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		EP146661A1	12/16/86	EPO				

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

	At-Speed Test Is Not Necessarlily An AC Test, by Jacob Savir and Robert Berry, Int'l Test Conf. 1991.
	IBM Technical Disclosure Bulletin 8-86 P. 1234-1236, Measuring Process-Induced AC Chip Performance Variations Using SRLs.
	IBM Technical Disclosure Bulletin 3-88 P. 288, Process Monitoring For LSSD Designs.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.